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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,050	06/26/2001	Harold Kutz	CYPR-CD00199	4196

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WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, CA 95113

EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,050	KUTZ ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-22 of this application. For example, the provisional application lacks support for all the features recited in independent claim 1, such as a wirebond pad, a circuit including an analog circuit and a digital circuit, and a switching circuit that selectively connects at least one of the analog input, analog output, digital input, and digital output to the wirebond pad under control of the processor.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 18 (*see* Fig. 1). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim2-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 2-6 recite the limitation "The apparatus" in line 1 of each claim. There is insufficient antecedent basis for this limitation in the claims. It is recommended that applicant review each of claims 7-22 for recitation of the limitation "The apparatus" and make changes, where appropriate, to be consistent with any changes made to claims 2-6.

6. It is recommended that applicant review claim 20 with regard to the recitation of "the digital output" in line 2 and "the digital input" in line 3. Does applicant intend for claim 20 to read "wherein the *digital output* is switched by an input to the multiple input logic gate" in line 3?

7. Dependent claims 7-22 inherit the indefiniteness of claim 6.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,356,958 to Lin.

With regard to claim 1, Lin discloses a microcontroller including: a circuit including an analog circuit (Fig. 3, item 306) and a digital circuit, (Fig. 3, item 304 or 306) where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (Fig. 3, items 312 and 374); a wirebond pad (Fig. 3, items 344, 324, and 340); a processor (Fig. 3, items 348, 356, and 364); and a switching circuit (Fig. 3, items 310) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the wirebond pad under control of the processor.

With regard to claim 3, Lin discloses the apparatus where the digital circuit includes a configurable digital circuit block (column 7, lines 6-8).

Therefore, Lin reads on the invention as claimed.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,509,758 to Piasecki, et al. ("Piasecki") in view of *Wirebonding: Reinventing the Process for MCMs* by H.K. Charles, et al. ("Charles").

With regard to claim 1, Piasecki discloses a microcontroller including: a circuit including an analog circuit (Fig. 1, item 22; column 3, lines 39-42) and a digital circuit, (Fig. 1, item 18) where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (*see generally*, Fig. 1 and column 3, lines 39-42); a pad (Fig. 1, item 12); a processor (Fig. 1, item 18); and a switching circuit (Fig. 1, items 14) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the pad under control of the processor.

With regard to claims 17-21, Piasecki discloses the apparatus where the switching circuit includes a tristate logic gate coupling the digital input to the pad, and where the digital input is switched by tristate control of the tristate logic gate; where the tristate logic gate includes an inverter; where the tristate logic gate includes a buffer; and where the multiple input logic gate includes a NAND gate (*see generally*, Fig. 2 and the accompanying text).

Piasecki does not expressly disclose a wirebond pad, as recited in independent claim 1. Charles discloses the use of wirebonding. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the wirebonding of Charles with the pad of Piasecki. The suggestion or motivation for doing so would have been to increase quality and reliability of the pads (page 300, paragraph 1, lines 5-8).

Therefore, it would have been obvious to combine Charles with Piasecki to obtain the invention as specified in claims 17-21.

12. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,555,452 to Calloway, Jr., et al. ("Calloway") in view of Charles.

With regard to claim 1, Calloway discloses a microcontroller including: a circuit including an analog circuit (Fig. 3, V_{in}) and a digital circuit, (Fig. 3, item 167) where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (*see generally*, Fig. 3 and column 3, lines 16-50); a processor (Fig. 3, item 157); and a switching circuit (Fig. 3, item 180) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the pad under control of the processor.

Calloway does not expressly disclose a wirebond pad, as recited in independent claim 1. Charles discloses the use of wirebond pads. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the wirebond pads of Charles with the circuit of Calloway. The suggestion or motivation for doing so would have been to increase quality and reliability of the circuit (page 300, paragraph 1, lines 5-8).

Therefore, it would have been obvious to combine Charles with Calloway to obtain the invention as specified in claim 1.

13. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,305,312 to Fornek, et al. ("Fornek") in view of Charles.

With regard to claim 1, Fornek discloses a microcontroller including: a circuit including an analog circuit (Fig. 1, items 116, 126, and 128) and a digital circuit, (Fig. 1, items 130 and 132) where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (*see generally*, Fig. 1); a processor (Fig. 1, item 137); and a switching circuit (Fig. 1, item 100) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the pad under control of the processor.

Fornek does not expressly disclose a wirebond pad, as recited in independent claim 1. Charles discloses the use of wirebond pads. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the wirebond pads of Charles with the circuit of Fornek. The suggestion or motivation for doing so would have been to increase quality and reliability of the circuit (page 300, paragraph 1, lines 5-8).

Therefore, it would have been obvious to combine Charles with Forneky to obtain the invention as specified in claim 1.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,768,337 to Kohno, et al. ("Kohno").

As described above with regard to the 35 U.S.C. 102(e) rejection of independent claim 1, Lin discloses all the features of claim 1. Lin does not expressly disclose the apparatus where the analog circuit includes a configurable analog circuit block.

Kohno discloses an apparatus where the analog circuit includes a configurable analog circuit block (column 12, lines 26-29). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Kohno with Lin. The suggestion or motivation for doing so would have been to realize multiple functions with one reconfigurable analog device by simply changing the circuit configuration into an optimal configuration depending on the operating mode of a system (column 1, lines 39-44).

Therefore, it would have been obvious to combine Lin with Kohno to obtain the invention as specified in claim 2.

15. Claims 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 5,107,146 to El-Ayat.

As described above with regard to the 35 U.S.C. 102(e) rejection of independent claim 1, Lin discloses all the features of claim 1. Lin does not expressly disclose all the features of dependent claims 7-22.

El-Ayat discloses the features of claims 7-22. For example, El-Ayat discloses the apparatus where the switching circuit includes an analog buffer amplifier (Fig. 1, items 22a, 22b, 22c, and 22d) in series with an analog switch (Fig. 1, item 24) coupling the analog output to the pads (Fig. 1, items 18e, 18f, 18g, and 18h), and where the analog

output is switched by the analog switch; where the switching circuit includes an analog switch (Fig. 1, item 24) coupling the analog output to the pads (Fig. 1, items 18e, 18f, 18g, and 18h), and where the analog output is switched by the analog switch; and where the switching circuit includes an analog switch (Fig. 1, item 24) coupling the analog input (Fig. 1, items 20a, 20b, 20c, and 20d) to the pads (Fig. 1, items 18a, 18b, 18c, and 18d), and where the analog input is switched by the analog switch.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine El-Eyat with Lin. The suggestion or motivation for doing so would have been to isolate the switch from the effects of the pads, and vice versa.

Therefore, it would have been obvious to combine El-Ayat with Lin to obtain the invention as specified in claims 7-22.

Response to Arguments

16. Applicant's arguments, see Amendment and Response to Office Action (pages 9-14), filed April 19, 2004, with respect to the rejections of claims 1, 3, and 5 under 35 U.S.C. 102(e) in view of Gauthier, et al., claims 1-22 under 35 U.S.C. 102(e) in view of Lesea, and claims 1, 2, and 4 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection are made in view of U.S. Patent Nos. 6,509,758 to Piasecki, et al., 6,356,958 to Lin, 5,555,452 to Callaway, Jr., et al., and 5,305,312 to Fornek, et al, 5,107,146 to El-Eyat, 6,768,337 to Kohno, et al., and in view of *Wirebonding: Reinventing the Process for MCMs* by H.K. Charles, Jr., et al.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM